RCA Application Note

AN-201

Application Considerations for RCA 3N98 and 3N99 Silicon MOS Transistors

by
D. M. Griswold

The unique characteristics of the new RCA 3N98 and 3N99 MOS (metal-oxide-semiconductor) transistors make them particularly useful in such applications as af and rf amplifiers, electrometers, and series and shunt chopper amplifiers. These silicon insulated-gate field-effect transistors, unlike junction-type field-effect devices and vacuum tubes, have a high input resistance which is independent of the polarity and magnitude of the applied bias voltage. This feature offers equipment designers a new degree of freedom in solid-state circuit designs. This note describes the operation and characteristics of these new MOS devices, and explains their use in various types of circuit configurations.

OPERATION OF MOS TRANSISTORS

A field-effect transistor contains a gate electrode whose sole purpose is to act as a charge-storage or control element. A charge placed upon this control element induces an equal but opposite charge in the channel beneath the gate. In most cases, the charge induced in the channel is free to contribute to conduction between the source and the drain.

If the channel is electrically conductive even in the absence of applied voltages, the transistor is called a *depletion* type. If the channel is conductive only when voltages are applied, the transistor is called an *enhancement* type. (The RCA 3N98 and 3N99 described in this note are depletion types.)

The control function is sometimes described by means of a depletion region which moves into or out of the channel and thus varies its cross-sectional area and resistance. However, this depletion region is merely the space-charge region required to terminate the gate's electric field. This charge storage by means of an electric field represents capacitance.

In the junction type of field-effect transistor, a p-n junction is used for the gate or control electrode, as shown in Fig.1. When this junction is reverse-biased, it functions as a charge-control capacitor: it allows only a small leakage current to flow and thus results in a high input resistance. This resistance is degraded only by its reasonably small, but temperature-sensitive, leakage current. Forward-bias operation

RADIO CORPORATION OF AMERICA
Electronic Components and Devices Harrison, N. J.

11-64

of this type of transistor is normally not desirable because the result is appreciable input current and unattractive power gain. This type of operation is analogous to the performance of a vacuum tube when its grid is biased positive relative to its cathode.

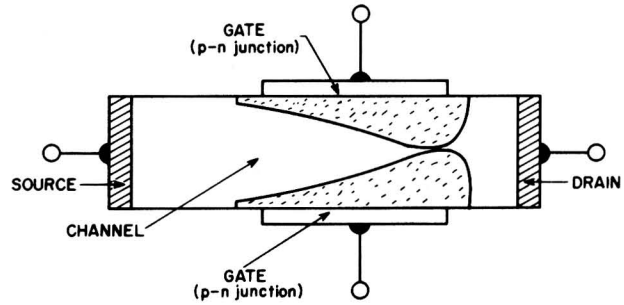

Fig.1 - Cross-sectional view of junction-type field-effect transistor.

The MOS type of field-effect transistor uses a metal gate electrode separated from the semiconductor material by a thin layer of silicon dioxide. Fig.2 shows a cross-sectional view of an MOS transistor using the depletion mode of operation. Like the p-n junction, the insulated gate can deplete the source-to-drain channel of its active carriers when

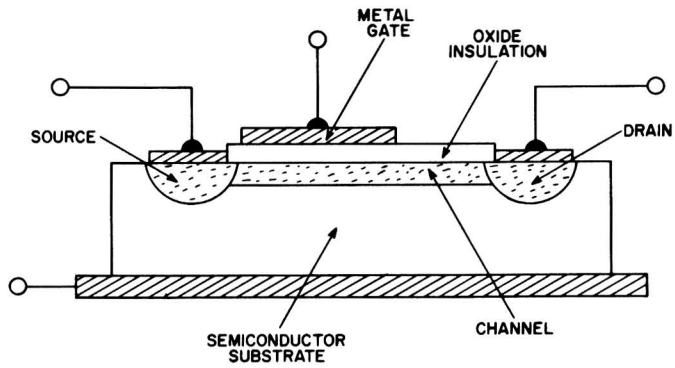

Fig.2 - Cross-sectional view of depletion-type MOS transistor.

appropriate bias voltages are applied. As is not the case for the p-n junction type, however, the conductivity of the MOS transistor channel can also be enhanced by altering the polarity of its gate-to-source voltage. Because the gate is well insulated and not rectifying, this unique mode of operation does not increase input current or reduce power gain. In addition, the leakage currents of the insulator are little affected by temperature changes, and are much lower than those of junction-type devices.

Fig.3 shows a cross-sectional view of an MOS transistor which operates entirely in the enhancement mode. As shown, the source and drain contact regions are separate and distinct diodes (the connecting channel

beneath the gate is removed), and the gate spans the region between the two diodes. When a positive bias voltage is applied to the gate*, electrons are drawn into the region beneath the gate. If sufficient voltage is applied, this region changes from p-type to n-type and provides a conduction path between the source and the drain. The device is normally cut off until the application of gate voltage permits conduction. Electrically, the increase in gate voltage is equivalent to a shift in the transfer characteristic along the gate-voltage axis. The importance of this device for switching applications appears appreciable.

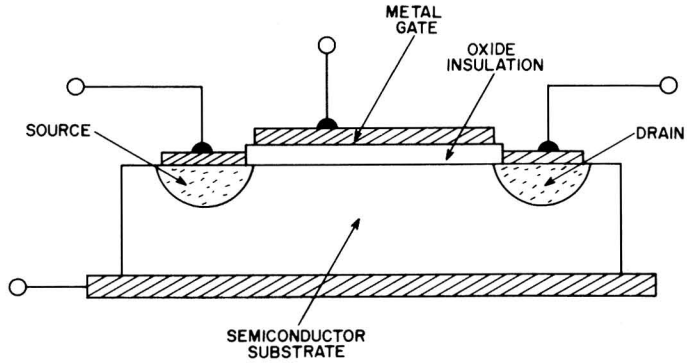

Fig.3 - Cross-sectional view of enhancement-type MOS transistor.

Circuit Symbol for MOS Transistor

Although there is as yet no official symbol for the MOS transistor, the symbol shown in Fig.4 represents some of the latest thinking on the part of industry.

In the MOS transistor, the *source and drain* regions form essentially ohmic contacts to the thin channel region. The *gate* control electrode takes the form of a metallic layer which is parallel to the channel and

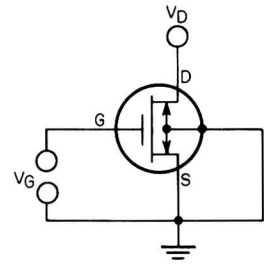

Fig.4 - Circuit symbol for MOS transistor.

separated from it by an insulating layer (silicon dioxide). The metal gate and the channel effectively form two plates of a capacitor, as depicted by the symbol.

Because the channel is formed on the surface of a semiconductor *substrate,* the substrate forms p-n junctions with the heavily diffused source and drain regions. These junctions act as back-to-back diodes in parallel with the channel, as shown in Fig.4. (An n-channel transistor is shown in Fig.4; for a p-channel device, the diodes would be reversed.)

* This discussion is based upon a device called an *n-channel* enhancement type in which channel conduction is by electrons. A similar device in which channel conduction is by holes is called a *p-channel* enhancement transistor.

The length and position of the gate in the symbol are also significant. All *enhancement-type* MOS transistors must have a full gate which extends all the way from source to drain. The *depletion-type* MOS transistor may have either a full gate or an offset gate, depending upon specific application requirements.

CHARACTERISTIC CURVE

Fig.5 shows the basic current-voltage relationships of an MOS depletion-type transistor operating in the common-source configuration. At low drain-to-source potentials and with the gate returned to source ($V_g = 0$), the channel resistance has the essentially ohmic character displayed in region A-B and current flows equally well in either direction.

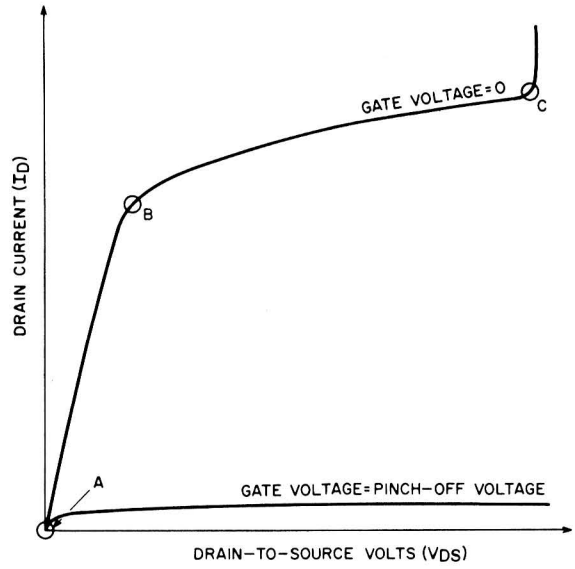

Fig.5 - Current-voltage characteristic curve for MOS transistor.

As the drain current is increased beyond point B, however, the IR drop in the channel produces a progressively greater voltage difference between the equipotential gate and those points in the channel successively closer to the drain. As this potential difference between gate and channel increases, the channel is depleted of carriers. The net effect is that the channel becomes "constricted" and any further increase in drain current is much more gradual. This condition leads to the description of region B-C as the "pinch-off" region. Beyond point C the transistor enters the "break-down region" and the drain current may increase excessively.

ELECTRICAL CHARACTERISTICS

The MOS transistor can take many forms, including p-channel and n-channel depletion or enhancement units; the insulated gate electrode may cover all or only a part of the source-to-drain channel. The 3N98 and 3N99 are n-channel depletion types in which the gate is offset for very

low feedback capacitance. Variations are almost innumerable but, in general, the equivalent circuit shown in Fig.6 can be applied to all MOS transistors operated in the channel pinch-off region. This circuit depicts MOS device operation from dc to signal frequencies approaching 100 megacycles; above this frequency, the case and leads begin to contribute inductive effects which are not included in the diagram. The equivalent circuit elements have the following significance:

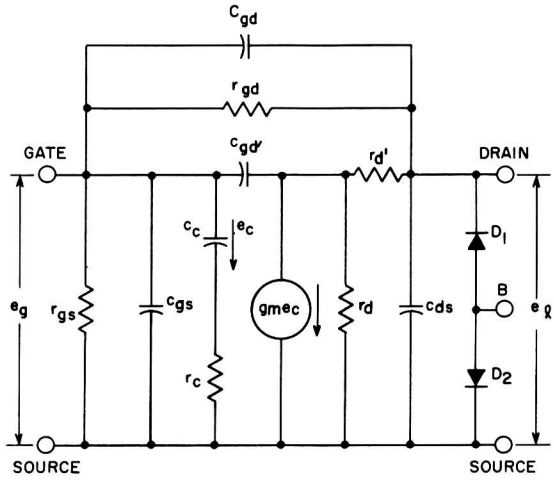

Fig.6 - Equivalent circuit for MOS transistor.

r_{gs} and r_{gd}. These resistances represent the leakage paths through and across the insulating oxide from gate to source and from gate to drain, respectively. In a properly fabricated MOS transistor, these leakage resistances are very high and the ratio between the two appears to be mainly a function of the relative physical distances across rather than through the silicon dioxide. In the 3N98 and 3N99 devices, the parallel combination of these resistances is greater than 10^{15} ohms.

In contrast to the junction type of field-effect transistor, whose gate current doubles for every eight or ten degrees centigrade increase in temperature, the typical MOS gate leakage remains below 10^{-13} ampere at 85° C.

c_C and r_C. The series network formed by c_C and r_C is a lumped approximation of the actual distributed network formed between the active channel resistance and the metalized gate. The sum total of the small capacitors distributed along the active channel resistance must charge and discharge through this resistance. Because the voltage across c_C performs the charge control, it is the important modulation parameter. The series resistance, r_C, is a lossy element; consequently, the high-frequency performance is a function of the time constant associated with r_C and c_C. The 3N98 has an equivalent c_C of about four picofarads and an r_C of one hundred ohms.

g_m and r_d. In the region beyond pinch-off, the drain current Id is relatively constant and suggests an equivalence to the constant-current generator, $g_m e_C$. At low frequencies, the intrinsic $g_m e_C$ and the extrinsic $g_m e_g$ are essentially equal. The dc g_m (transconductance) is represented

by the slope of the I_d/E_g transfer characteristic. Fig.7 shows such a characteristic curve for the 3N98.

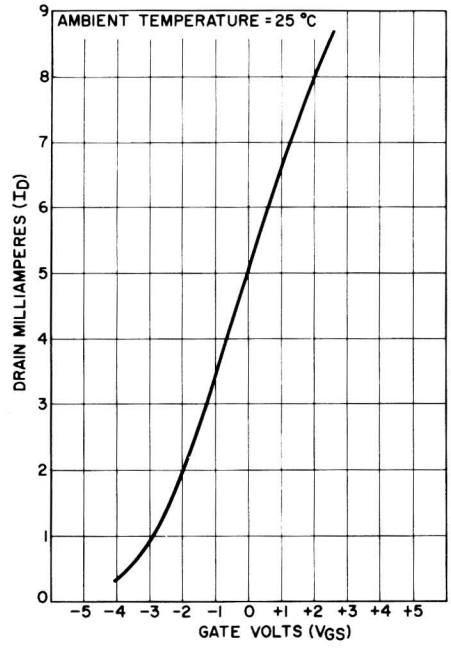

Fig.7 - Drain current as a function of gate voltage for the 3N98.

The resistor r_d in shunt with the generator represents the output resistance. Its value is given by the slope of the output characteristic curves, which are shown in Fig.8 for the 3N98 MOS transistor. As can be seen from this curve, r_d increases as the channel is further depleted

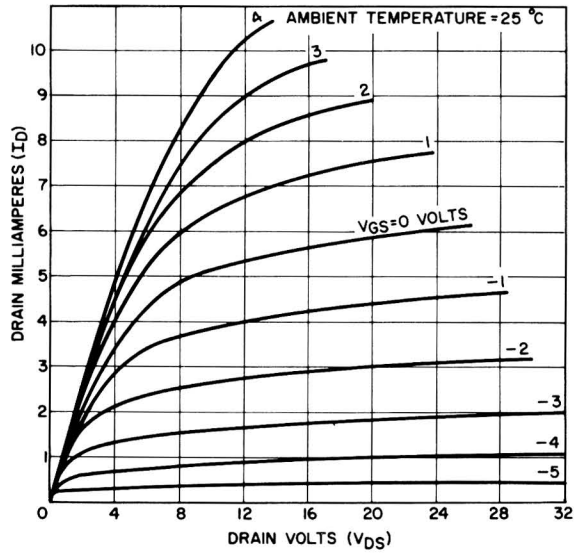

Fig.8 - Output characteristic curves for 3N98 MOS transistor.

and decreases significantly at low drain voltages when the channel conductivity is enhanced. As a result, at low drain-to-source voltages in a typical amplifier-type depletion MOS transistor, the output resistance

may be varied from a low value of about 300 ohms to as high as several hundred megohms by variation of the gate voltage.

r_d'. In a "full-gate" MOS transistor, r_d' approaches zero; in a partial- or offset-gate MOS type, however, r_d' represents the portion of the channel resistance which is not modulated by the insulated gate electrode. In such a unit, r_d' is simply a lossy element in series with the external load. In its favor, it should be noted that r_d' is a necessary byproduct of design considerations which result in reduced feedback capacitance and a higher drain-to-source breakdown voltage.

c_{gd}, c_{gs}, and c_{ds}. These terms represent the case and interlead capacitances between the gate and the drain, gate and source, and drain and source, respectively. The first two capacitances also include any non-voltage-dependent capacitances, such as capacitance caused by the physical overlap of the insulated gate over the source or drain. The capacitances related to D_1 and D_2 are included in the term c_{ds}.

c_{gd}'. The term c_{gd}' represents the intrinsic device gate-to-drain capacitance. In MOS transistors which have "full gates", c_{gd}' is relatively high (1 to 2 picofarads) because the gate metalizing covers the entire source-to-drain channel and slightly overlaps the drain diffusion. The value of c_{gd}' remains fairly constant in a "full-gate" device. In "partial-gate" devices such as the 3N98 and 3N99, however, the gate metalizing does not extend all the way to the drain, and c_{gd}' is significantly reduced, as shown in Fig.9. Because of this reduced c_{gd}' characteristic, the "partial" or offset-gate configuration is more desirable for high-gain voltage-amplifier applications that the "full-gate" MOS device.

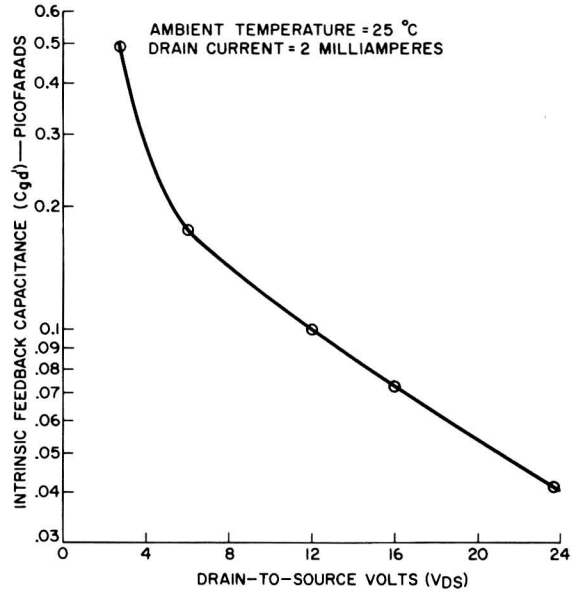

Fig.9 - Intrinsic feedback capacitance as a function of drain-to-source voltage.

D_1 and D_2. These diodes are formed by the junctions of the n^+ drain to the slightly p-type silicon substrate.

Substrate B. To some degree, the slightly p-type silicon substrate forms a p-n junction with the n-type channel and may act as a second

control electrode. Whether it actually does or not depends, among other things, on the channel length and the doping level of the substrate. In the 3N98 and 3N99, the substrate-to-drain transconductance ranges from 400 to 1000 micromhos.

The substrate gates of the 3N98 and 3N99 transistor are made accessible by the fourth lead. When a negative bias is applied between this substrate lead and the source lead, the drain current is decreased. For some applications, the substrate gate has the usual disadvantages associated with a silicon junction gate, i.e., a temperature-sensitive saturation current and low impedance when a positive bias is applied between substrate and source. Because the substrate transconductance is not closely controlled at present, the substrate lead should be ac-grounded and tied to a dc voltage so that the potential difference between substrate and gate is minimized. (RCA published data for the 3N98 and 3N99 include maximum ratings for insulated-gate-to-substrate-gate voltage).

CIRCUIT PERFORMANCE

Fig.10 shows the three basic single-stage amplifier configurations for MOS transistors: common-source, common-gate, or common-drain. Each

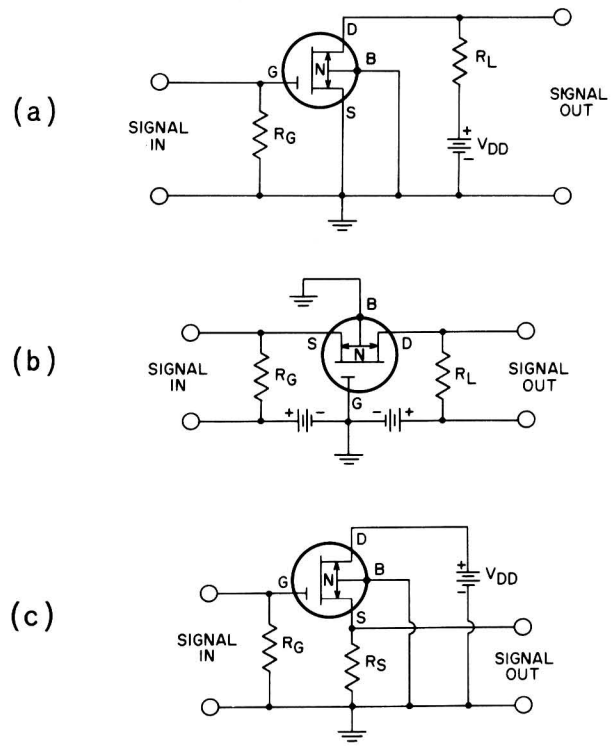

Fig.10 - (a) Common-source, (b) common-gate, and (c) common-drain single-stage amplifier configurations for MOS transistors.

has its own particular advantages over others for use in specific applications.

The common-source arrangement is most frequently used and features high input impedance, medium to high output impedance, and voltage gain

greater than unity. In this mode of operation, the input signal is applied between gate and source and the output signal is taken between drain and source. The *common-source voltage gain without feedback*, A, may be determined by use of the following equation:

$$A = \frac{g_m r_d R_L}{r_d + R_L} \tag{1}$$

where g_m is the gate-to-drain transconductance, r_d is the drain resistance, and R_L is the composite load resistance. An unbypassed source resistor produces negative feedback proportional to the output current. *The common-source voltage gain with an unbypassed source resistor*, A^1, can be expressed as follows:

$$A^1 = \frac{g_m r_d R_L}{r_d + (g_m r_d + 1) R_S + R_L} \tag{2}$$

where R_S is the unbypassed source resistance. The common-source output impedance, Z_o, is increased by the unbypassed source resistor, as given by:

$$Z_o = r_d + (g_m r_d + 1) R_S \tag{3}$$

The common-drain arrangement is also frequently referred to as a source-follower. In this mode, the input impedance is higher than in the common-source configuration, the output impedance is low, there is no polarity reversal between input and output, the voltage gain is always less than unity, and distortion is low. The source-follower is used in applications which require reduced input-circuit capacitance, downward impedance transformation, or increased input-signal-handling capability. As shown in Fig.10, the input signal is effectively injected between gate and drain and the output is taken between source and drain. The circuit inherently has 100-per-cent negative voltage feedback; its gain A^1 may therefore be written as follows:

$$A^1 = \frac{R_S}{\left(\frac{\mu + 1}{\mu}\right) R_S + \frac{1}{g_m}} \tag{4}$$

Because the amplification factor μ is usually very much greater than unity in an MOS transistor, this equation can normally be simplified as follows:

$$A^1 \approx \frac{g_m R_S}{1 + g_m R_S} \tag{5}$$

If it is assumed that the transistor g_m is 2000 micromhos and the R_S is 500 ohms, the stage gain A^1 is 0.5. With the same R_S and a transistor g_m of 10,000 micromhos, the stage gain only increases to 0.83.

If the resistor R_G is returned to ground as shown in Fig. 10, the input resistance R_i of the stage is equal to R_G. If, however, R_G is returned to the source terminal, the effective input resistance R_i' may be determined from the following equation:

$$R_i' = \frac{R_G}{(1 - A')} \tag{6}$$

where A' is the voltage amplification of the stage having feedback. For example, if R_G = 1 megohm and A' = 0.5, R_i' = 2 megohms.

If the load is resistive, the effective input capacitance C_i' of the source-follower is reduced by the inherent voltage feedback and is given by

$$C_i = c_{gd} + (1-A')c_{gs} \quad (7)$$

For example, with a typical 3N99 having a c_{gd} of 0.3 picofarad and a c_{gs} of 5 picofarads and if A' is equal to 0.5, then C_i' is reduced to 2.8 picofarads.

The source-follower output resistance R_o' is given by

$$R_o' = \frac{r_d R_S}{(g_m r_d + 1)R_S + r_d} \quad (8)$$

where r_d is the transistor drain-to-source resistance in ohms. With a 3N99 having a g_m of 2000 microhmos, r_d of 7500 ohms, and R_S of 500 ohms, R_o' is equal to 241 ohms.

The source-follower output capacitance C_o' may be expressed as follows:

$$C_o' = c_{ds} + c_{gs}\,[(1-A')/A'] \quad (9)$$

If A' is equal to 0.5 (as assumed for the sample input-circuit calculations), it can be seen that C_o' would reduce to the sum of c_{ds} and c_{gs} (1.5 + 5.0 = 6.5 picofarads). This figure is typical for a 3N99 used with a total external source resistance of 500 ohms. If the same 3N99 is used with an external source resistance of 2000 ohms, A' has a value of 0.8 and C_o' drops to 2.87 picofarads.

The common-gate circuit shown in Fig.10 is used to transform from a low input impedance to a high output impedance. The input impedance of this configuration has approximately the same value as the output impedance of the source-follower circuit. The common-gate circuit is also a desirable configuration for high-frequency applications because its relatively low voltage gain makes neutralization unnecessary in most instances. The general expression for *common-gate voltage gain, A,* is given by

$$A = \frac{(g_m r_d + 1)R_L}{(g_m r_d + 1)R_G + r_d + R_L} \quad (10)$$

where R_G is the resistance of the input signal source. If typical 3N99 values are assumed (g_m = 2000 micromhos, r_d = 7500 ohms, R_L = 2000 ohms, and R_G = 500 ohms), the common-gate voltage gain is 1.8. Doubling the value of R_G reduces the voltage gain to 1.25.

The MOS transistor may also be used in a number of different two-stage cascade arrangements either with other MOS transistors or with bipolar transistors or vacuum tubes. The circuit shown in Fig.11 uses two 3N99 transistors and, with a load impedance of 1000 ohms, produces an over-all voltage gain of approximately 10. The first stage has a voltage gain of about 20 because, at the reduced drain current level resulting from the dc self-bias of the source resistor, the g_m/I_d ratio is substantially improved over the zero-gate-voltage condition. In addition, the reduction of the first-stage drain current to the 100-microampere level permits the relatively large 0.1-megohm dc load resistance to be used without an excessive drop in the quiescent drain-to-source voltage. The high input impedance presented by the second 3N99 in turn prevents undesirable loading of the first stage. The low output impedance from the pair is

then obtained by operating the second stage as a source-follower having a voltage gain of 0.5.

The circuit of Fig.12 shows the use of direct coupling between two MOS transistors. This circuit is similar to the one shown in Fig.11 in that the first stage is operated at a reduced level of drain current for a voltage gain of about 20 and the second stage is designed as a source-follower to allow for low output impedance. However, because all coupling capacitors have been removed, an additional bias battery must be used with the first-stage gate to accomplish what the bypassed source resistor did in the circuit in Fig.11. The main drawback associated with the missing source resistor is that the temperature stability of the stage is reduced and closer control of the ambient conditions is required.

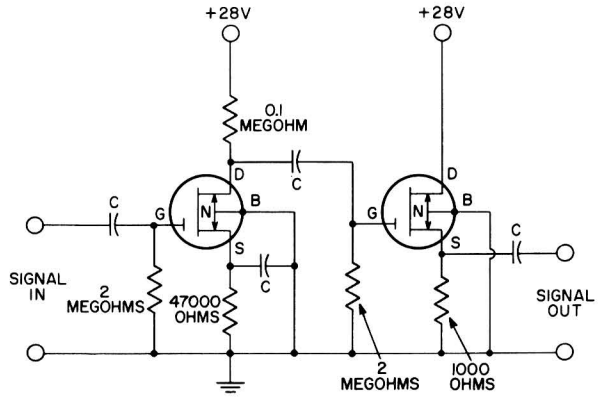

Fig.11 - MOS transistors in R-C coupled cascade.

In the circuit of Fig.12, it is interesting to note that although the drain voltage of the first stage is applied directly to the second-stage gate, its effect is partially cancelled by the increased voltage

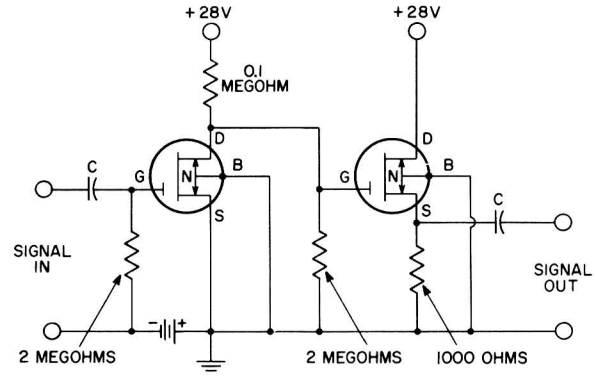

Fig.12 - MOS transistors in direct-coupled cascade.

drop across the 1000-ohm source resistor caused by the enhanced second-stage drain current. As an example, if the quiescent drain current of the second stage is 6 milliamperes (at $V_{GS} = 0$), the second-stage gate has -6 volts bucking +12 volts, or a net positive potential of 6 volts. This

potential enhances the drain-current flow, and causes a greater voltage drop across the second-stage source resistor so that the gate is balanced at about half the original difference, or 3 volts (for a unit in which $g_m = \frac{1}{R_S}$).

The circuit of Fig.13 uses the 3N98 MOS transistor to drive the low input impedance of an n-p-n power transistor. The circuit shown uses the 3N98 in the common-source rather than the source-follower configuration to obtain the largest possible gain (about 0.4). If minimum distortion

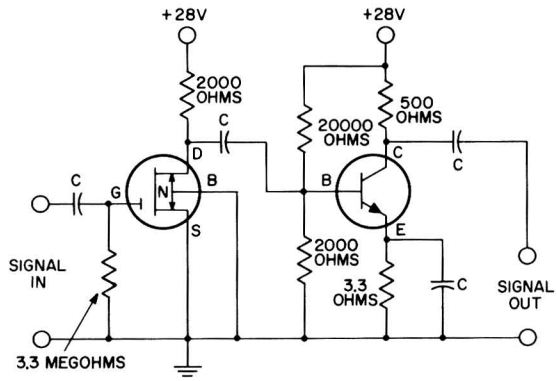

Fig.13 - MOS transistor driving bi-polar power transistor.

were the prime consideration, the 3N98 would be used as a source-follower at a sacrifice in voltage gain of 30 to 50 per cent. In either configuration, the MOS transistor is used entirely as a high-to-low impedance transformer. Even though the low input impedance of the conventional power transistor limits the voltage gain obtained from the first stage, the first-stage power gain can be very high because of the very large impedance ratio which may be obtained from the MOS transistor.

The use of an MOS transistor as a voltage-controlled attenuator is based on the nature of its output characteristics at low drain-to-source potentials (the ohmic region). Variation of the gate voltage of the transistor causes the drain-to-source resistance to increase or decrease, but the IR relationship of this resistance remains essentially linear. The primary advantages of the MOS transistor in voltage-controlled attenuator circuits are the very small gate power requirements and the wide dynamic range.

Fig.14 shows r_d as a function of gate voltage for a typical 3N98 (n-channel depletion-type) transistor. This characteristic may be applied in a simple L-pad arrangement in which the transistor serves as the variable resistance in the low side of the attenuator. In this type of circuit (illustrated in Fig.15), the maximum attenuation is normally between 60 and 70 db and the minimum signal reduction is 1 or 2 db. Proper performance of this circuit is possible only when the attenuator unit is followed by a high-impedance load such as a common-source MOS transistor amplifier.

In another version of the L-pad attenuator, the MOS transistor is placed in the series arm. In this instance, the shunt arm must have low

impedance if the useful maximum attenuation figure of 60 to 70 db is desired. The minimum attenuation normally would be between 1 and 6 db.

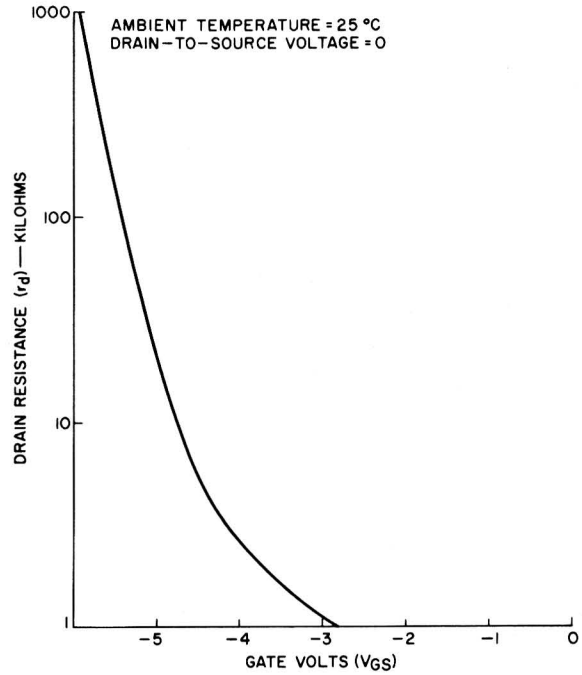

Fig. 14 - MOS transistor "ohmic" resistance as a function of gate voltage.

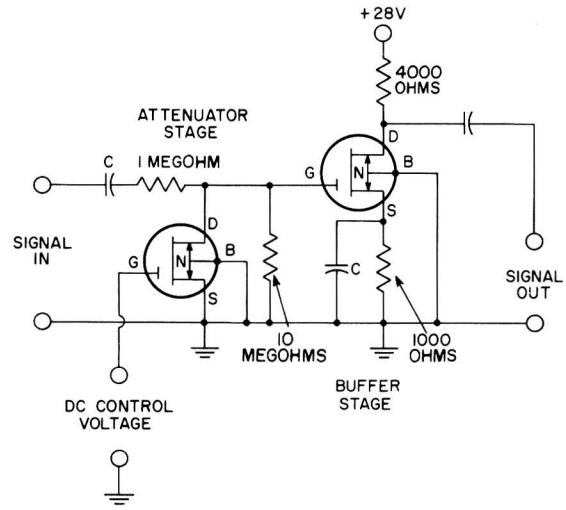

Fig. 15 - MOS transistor used in L-pad attenuator circuit.

HANDLING CONSIDERATIONS

As previously mentioned, one of the outstanding features of the MOS transistor is its very high input resistance, which in many cases is even higher than that of the best electron tubes. However, unlike the electron tube, whose control element (grid) operates in a vacuum, the MOS tran-

sistor depends on the relative perfection of a very thin glass layer (SiO_2) between its control electrode (gate) and the active channel. If this layer is punctured by the inadvertent application of excess voltage to the external gate connection, the damage is irreversible. If the damaged area is small enough, the additional leakage may not even be noticed in the majority of circuits. Greater damage may degrade the device to the leakage levels associated with a junction-gate transistor. It is very important, therefore, to take appropriate precautions to insure that MOS transistor gate-voltage ratings are not exceeded.

Static electricity represents the greatest threat to the gate insulation in the MOS transistor. A large electrostatic charge can accumulate on the gate electrode if the transistor is allowed to slide around in plastic containers or if the leads are brushed against fabrics such as silk or nylon. This type of charge accumulation can be avoided completely by wrapping the leads in conductive foils, by use of conductive containers, or by otherwise electrically interconnecting the leads when the transistors are being transported.

A second cause of electrostatic charge damage to the gate insulation can be traced to the people who handle the transistors. A human being is said to have a capacitance of about 150 picofarads. Nearly everyone has noticed the spark which jumps from his hand to a lamp or other metal fixture on a cold dry day. This spark represents a discharge of several thousand volts and is associated with relative humidity levels of about 10 per cent or less. At relative humidity levels of 35 per cent, a person may accumulate an electrostatic potential of 300 volts. If an individual in this charged condition grasps an MOS transistor by the case and plugs it into a piece of test equipment, or in any other way causes the gate lead to contact "ground" before the other leads do, there is a good chance that his accumulated electrostatic charge may break down the gate insulation. The best way to prevent this type of damage is to use a simple electrostatic grounding strap during all handling of these transistors. Such a grounding strap may have an impedance to ground of several megohms and still accomplish the primary purpose of "leaking off" static electricity.

In the majority of applications, associated circuit impedances are low enough to prevent any accumulation of electrostatic charge. Thus, although the gate insulation may be damaged by improper handling of the transistor before it is connected into an actual circuit, thousands of hours of operation under practical circuit conditions have shown that the gate insulation is quite reliable under long-term stress within published ratings.